RESEARCH ARTICLE OPEN ACCESS

Total Harmonic Distortion Analysis of Three Phase Nonlinear Load Using H-Bridge Vsi Topology Based_ Dstatcom

T. Santosh Kumar[1], Dr. K. B. Madhu Sahu[2], Ch. Krishna Rao[3]
[1] M.Tech Scholar, Dept. of EEE, AITAM Engineering College, A.P., India
[2] Professor, Dept. of EEE, AITAM Engineering College, A.P., India
[3] Assoc. Prof., Dept. of EEE, AITAM Engineering College, A.P., India

ABSTRACT
This paper presents the detailed model, control and simulation of H-Bridge VSI topology based DSTATCOM. It also describes the control of multilevel inverter supplied by Photovoltaic system and a battery bank which is connected to the supply system. It is well known that the Power Quality of the Multililevel Inverter signals depends upon the number of levels. Basic structure and operating principle of the Cascaded H-Bridge Multilevel Inverter are explored. The phase shifted SPWM is used for reducing the lower order harmonics of the output voltage and the Park's transformation is employed to decouple the active and reactive power components for regulating the compensation power. The controller equations are such that the phase shifted SPWM pulses are generated automatically for any number of levels. The effectiveness of the proposal method is evaluated in simulation by using Matlab/Simulink. The results of the simulation are analyzed and discussed.
***Keywords*:** PV Cell, DSTATCOM, Power Quality Level shifted Pulse width modulation (LSPWM), Phase shifted Pulse width modulation (PSPWM), Proportional-Integral (PI) control, Voltage source inverter (VSI).

I. INTRODUCTION

Solar photovoltaic (PV) system generates electricity with advantages such as no pollution, no noise and many more. Solar PV is well suited to remote or arid regions. Nowadays solar power is the quite essential energy source and receiving considerable attention from the researchers. The rapid evolution of semiconductor devices manufacturing technologies and the designer's orientation has enabled the development of new structures of converters (inverters) with a great performance compared to conventional structures. So, these new technologies of semiconductor are more suited to high power applications and they enable the design of multilevel inverters. The main advantage of multilevel inverters is that the output voltage can be generated with a low harmonics. Thus it is admitted that the harmonics decrease proportionately to the inverter level. For these reasons, the multilevel inverters are preferred for high power applications. However, there is no shortage of disadvantages. Their control is much more complex and the techniques are still not widely used in industry.

One of the most common power quality problems today is voltage sags. Voltage sag is a short time (10 ms to 1 minute) event during which a reduction in r.m.s voltage magnitude occurs. It is often set only by two parameters, depth/magnitude and duration. The voltage sag magnitude is ranged from 10% to 90% of nominal voltage (which corresponds to 90% to 10% remaining voltage) and with a duration from half a cycle to 1 min. In a three-phase system voltage sag is by nature a three-phase phenomenon, which affects both the phase-to-ground and phase-to-phase voltages. Voltage sag is caused by a fault in the utility system, a fault within the customer's facility or a large increase of the load current, like starting a motor or transformer energizing. Typical faults are single-phase or multiple-phase short circuits, which leads to high currents. The high current results in a voltage drop over the network impedance. At the fault location the voltage in the faulted phases drops close to zero, whereas in the non-faulted phases it remains more or less unchanged.

The STATCOM used in distribution systems is called DSTACOM (Distribution-STACOM) and its configuration is the same, but with small modifications. It can exchange both active and reactive power with the distribution system by varying the amplitude and phase angle of the converter voltage with respect to the line terminal voltage.

A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. There are several types of multilevel inverters: cascaded H-bridge (CHB), neutral point clamped, flying capacitor. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. CHB inverters can also

increase the number of output voltage levels easily by increasing the number of H-bridges. This paper presents a DSTATCOM with a proportional integral controller based CHB multilevel inverter for the harmonics and reactive power mitigation of the nonlinear loads. This type of arrangements have been widely used for PQ applications due to increase in the number of voltage levels, low switching losses, low electromagnetic compatibility for hybrid filters and higher order harmonic elimination.

II. PHOTOVOLTAIC SYSTEM

The Electrical equivalent circuit model of PV cell consists of a current source in parallel with diode as shown in figure. The PV cell characteristics are strongly nonlinear in nature; The Related expression is given in equation (1) as follows:

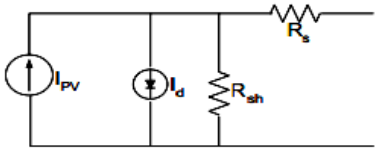

Fig.1. Equivalent circuit of solar PV

$$I = I_{PV} - I_0\left[e^{\frac{q\,V+IR_S}{AKT}} - 1\right] - \frac{V+IR_S}{R_{SH}} \quad (1)$$

Where,

I_{PV}	Photo-generated current (A)
I	Cell output current (A)
I_d	Diode Saturation Current (A)
V	Cell Output Voltage (V)
R_s	Series Resistor (Ω)
e	Electron Charge 1.6×10-19 (coulombs)
K	Boltzman Constant (j/K)
T	cell temperature

The block diagram of PV system shown in Fig.2. It consists of a DC-DC converter multilevel inverter and a battery bank.

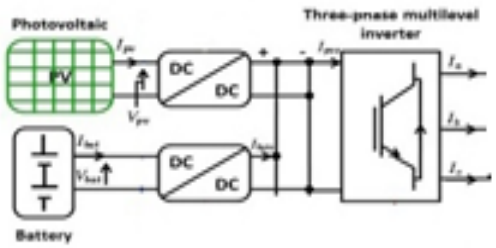

Fig.2. Block diagram of PV system

III. DIODE CLAMPED MULTILEVEL INVERTER

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m-level diode-clamp inverter needs m-1 capacitors on the dc bus. A single-phase five-level diode-clamped inverter, which can produce a nine-level phase to phase voltage waveform, is shown in Fig.3. The Insulated Gate Bi-Polar transistors are used as switches.

The IGBT has the output switching and conduction characteristics of a bipolar transistor but is voltage-controlled like a MOSFET. In general, this means it has the advantages of high-current handling capability of a bipolar with the ease of control of a MOSFET. However, the IGBT still has the disadvantages of a comparatively large current tail and no body drain diode.

The dc bus consists of four capacitors, i.e., C_1, C_2, C_3, and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. DCMI output voltage synthesis is relatively straightforward. To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage

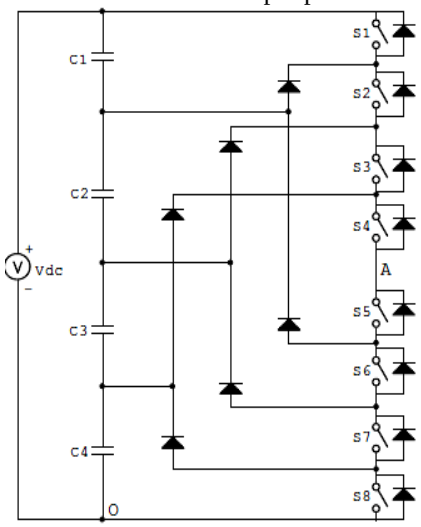

Fig.3. A single-phase five-level diode-clamped inverter.

Reference point. Using the five-level inverter shown in Fig.3, there are five switch combinations to generate five level voltages across A and O. Table: 1 shows the phase voltage level and their corresponding switch states. In the Table, state 1 represents that the switch is ON, and state 0 represents the switch is OFF. There exist four complementary switch pairs in each phase, i.e., S_1-S_5, S_2-S_6, S_3-S_7 and S_4-S_8.

Table: 1 Diode-clamped five-level inverter voltage levels and their switch states.

Output V_{A0}	Switch State							
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1 = 0$	0	0	0	0	1	1	1	1

IV. DESIGN OF MULTILEVEL TOPOLGY BASED DSTATCOM

4.1 Principle of DSTATCOM

A DSTATCOM (Distribution Static Compensator), which is schematically depicted in Fig.4, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

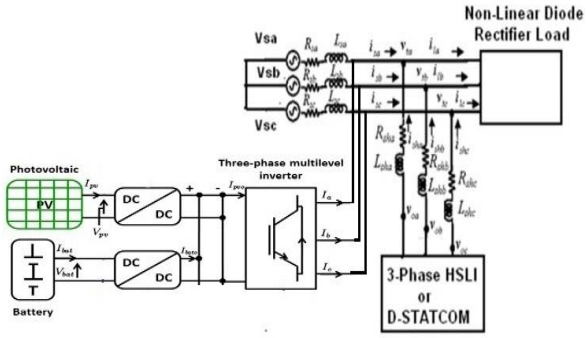

Fig.4. Schematic diagram of DSTATCOM

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power
2. Correction of power factor
3. Elimination of current harmonics.

4.2 Control Strategy

4.2.1 Reference current generator

The Control block diagram of the DSTATCOM is shown in Fig.5. V_1 is the instantaneous three phase source voltage.I_L is the instantaneous three phase set of measured current at load. These two quantities first to be transformed to the stationary two axes (α-β) co-ordinates. The instantaneous real and instantaneous reactive power p and q are determined using equations (2) and (3).

$V_{\alpha\beta}$ = [C] [Vsabc] (2)

$I_{\alpha\beta}$ = [C] [I_{Labc} (3)

Where

$$C = \sqrt{(2/3)}\begin{bmatrix} 1 & -1/2 & 1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}$$

$p = V\alpha\, I\alpha + V\beta\, I\beta$ (4)

$q = V_\alpha I_\beta - V_\beta I_\alpha$ (5)

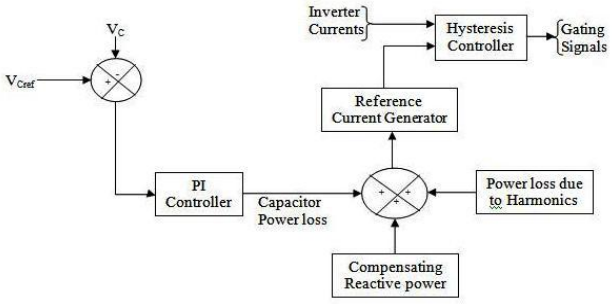

Fig.5. Block diagram of control circuit

The real power consists of fundamental and harmonic components. The harmonic components of real power (p) can be separated by using high pass filter. The DC capacitor voltage is compared with the DC reference voltage V_{dc} by using PI controller. The output of the PI controller represents the losses at the capacitor.

$$\begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} = \begin{bmatrix} V_{S\alpha} & V_{S\beta} \\ -V_{S\beta} & V_{S\alpha} \end{bmatrix} \begin{bmatrix} p^* \\ q^* \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = [C]^T \begin{bmatrix} i_\alpha^* \\ i_\beta^* \end{bmatrix} \quad (7)$$

4.2.2 Hysteresis Controller

The hysteresis current controller compares the three phase reference currents (i_{ca}^*, i_{cb}^*, i_{cc}^*) generated using equation (7) with actual inverter currents (i_{ca}, i_{cb}, i_{cc}) and generates the switching pulses to the inverter.

4.3 Cascaded H-Bridge Multilevel Inverter

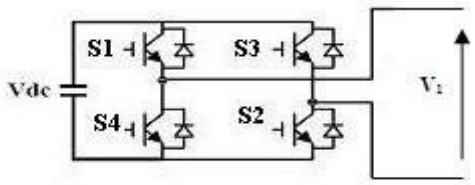

Fig.6. Circuit of the single cascaded H-Bridge Inverter

Fig.6 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+1 and voltage step of each level is given by Vdc/2n, where n is number of H-bridges connected in cascaded. The switching table is given in Table: 2.

Table: 2 Switching table of single CHB inverter

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

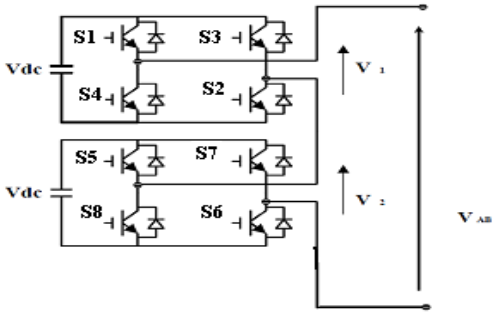

Fig.7. Block diagram of 5-level CHB inverter model

The switching mechanism for 5-level CHB inverter is shown in Table: 3.

Table: 3 Switching table for 5-level CHB Inverter

Switches Turn On	Voltage Level
S1, S2	Vdc
S1,S2,S5,S6	2Vdc
S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

4.4 PWM techniques for CHB Inverter

The most popular PWM techniques for CHB inverter are;

1. Phase Shifted Carrier PWM (PSCPWM)
2. Level Shifted Carrier PWM (LSCPWM).

4.4.1 Phase Shifted Carrier PWM (PSCPWM)

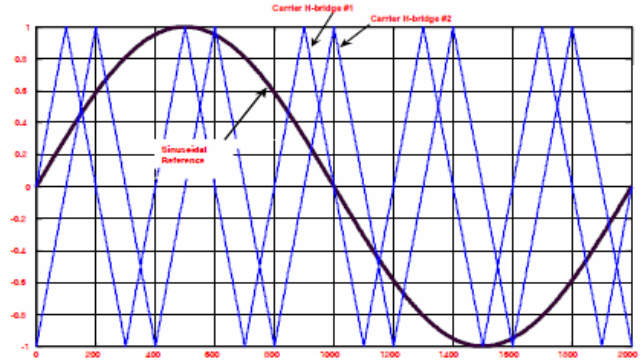

Fig.8. Phase Shifted Carrier PWM

Fig.8 shows the Phase shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier phase shift of 180°/m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

4.4.2 Level Shifted Carrier PWM (LSCPWM)

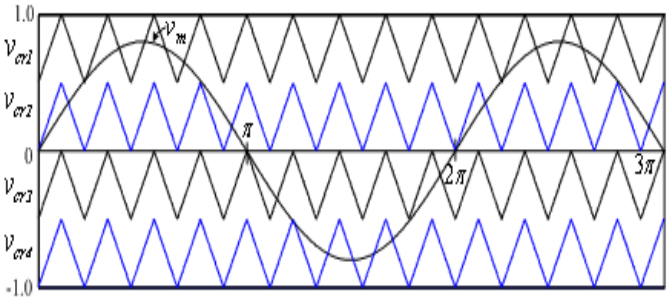

Fig.9. Level shifted carrier PWM

Fig.9 shows the Level shifted carrier pulse width modulation. Each cell is modulated independently using sinusoidal unipolar pulse width modulation and bipolar pulse width modulation respectively, providing an even power distribution among the cells. A carrier Level shift by 1/m (No. of levels) for cascaded inverter is introduced across the cells to generate the stepped multilevel output waveform with lower distortion.

V. SIMULATION RESULTS

The performance of the proposed control strategies was evaluated by computer simulation using MATLAB. Fig.10 shows the simulated system

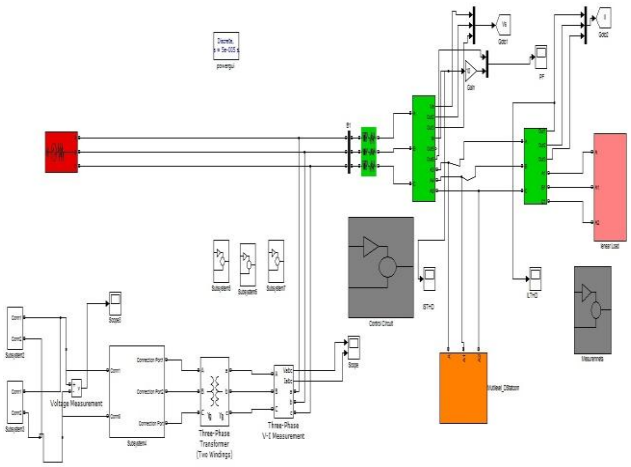

Fig.10. Matlab/Simulink power circuit model

5.1 Linear load without DSTATCOM

Fig.11 shows the Source voltage and source current waveform of linear load without DSTATCOM. From this output we can observe that voltage and current waves are not in same phase. The current waveform is lags the voltage waveform. This is due to inductive load at the load terminal. The presence of reactive load reactive power disturbances occur in the supply system. The imbalance in reactive power reduces the power factor.

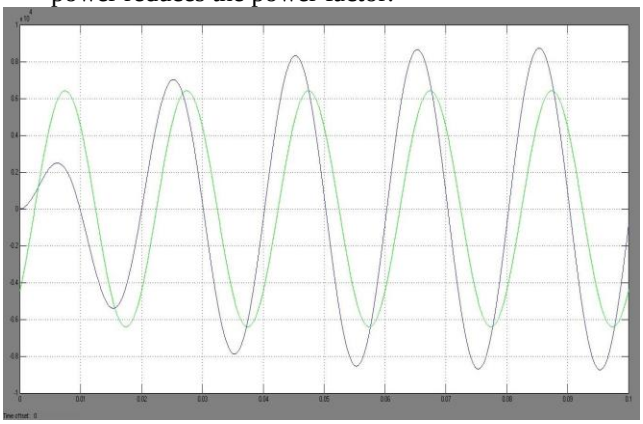

Fig.11. PF Output for linear load without DSTATCOM

5.2 Linear load with DSTATCOM

Fig.12 shows the source voltage and current waveforms for linear load with DSTATCOM. The voltage and current waveforms are in same phase. The shunt compensating devices presented at load end supplies the required reactive power to the load and maintains the power factor unity.

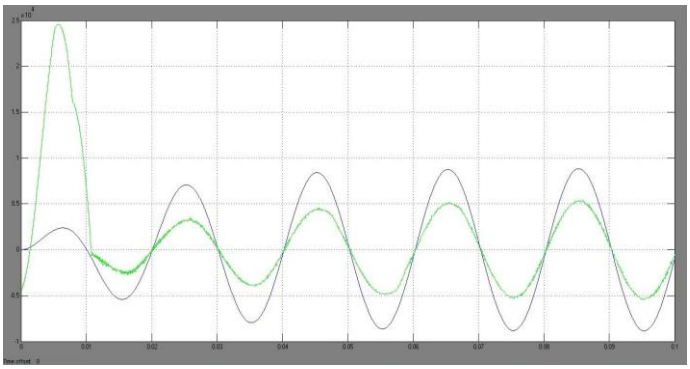

Fig.12. PF Output for linear load with DSTATCOM

5.3 Nonlinear load without DSTATCOM

Fig.13 represents the source voltage, source current and load current waveforms. The nonlinear loads at load end introduce harmonics in supply system. The presence harmonics introduces power quality problems. This hormonics makes the source current and load current wave forms non sinusoidal.

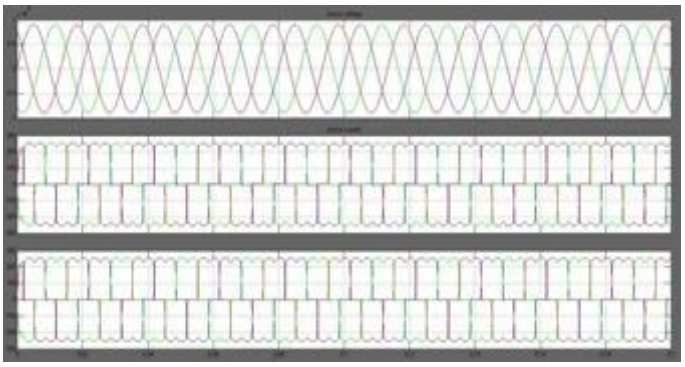

Fig.13. V_S, I_S & I_L outputs for the model nonlinear load without DSTATCOM

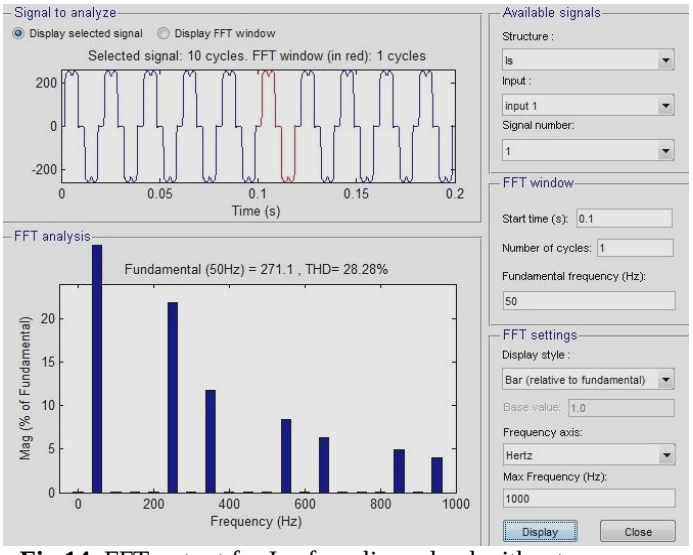

Fig.14. FFT output for I_S of nonlinear load without DSTATCOM

From Fig.14 we can observe that for nonlinear loads without DSTATCOM we can get THD as 28.28%.

5.4 Non linear load with DSTATCOM

Fig.14 represents the source voltage, source current, load current waveforms. The shunt compensating device DSTATCOM connected at load terminals .Which makes the source current sinusoidal. By using multilevel DSTATCOM we can reduces the source harmonics.

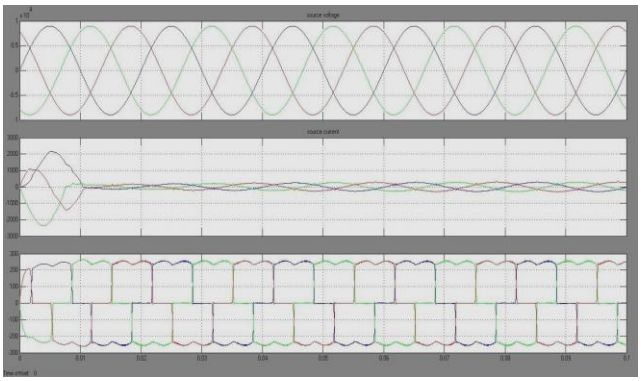

Fig.15. V_S, I_S & I_L outputs for the model nonlinear load with DSTATCOM

Fig.16 shows the FFT analysis of source current for the model nonlinear load with DSTATCOM.

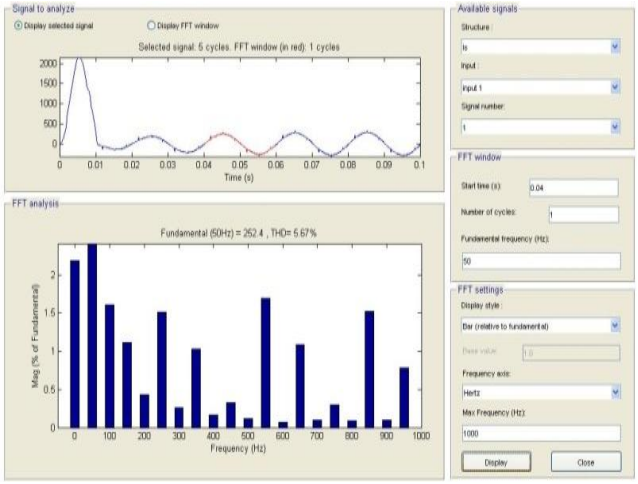

Fig.16. FFT output for I_S of nonlinear load with DSTATCOM

From this output we can observe that for nonlinear loads by using DSTATCOM we can reduce THD as 5.26%.

VI. CONCLUSION

This paper studied a five level Cascaded H-bridge inverter Topology based DSTATCOM. The effectiveness of reactive power compensation and harmonic reduction for the multilevel DSTATCOM is demonstrated in a power system with linear and nonlinear loads. The simulation results validate the performance of DSTATCOM for both reactive power compensation as well as harmonic reduction functionality to mitigate the power quality issues thus increases the utilization factor of the system.

REFERENCES

[1] Tzeng-Shong Yeh, Huang-Fu Jhu and Hsiao-Wei Sung, "Modelling and Control of 3-Phase Multilevel Inverter-based STATCOM", IEEE Trans. Power Electron., 2010.

[2] B.Housseini, R.Beguenane, F.A.Okou and M.A.Tankari, "Advanced Multilevel Control Strategy for Induction Motor Drive Utilization of PV-Battery Standalone System and Total Harmonic Distortion Analysis", IEEE Trans. Power Electron., 2012.

[3] K.A Corzine, and Y.L Familiant, "A New Cascaded Multi-level H-Bridge Drive," IEEE Trans. Power.Electron., vol.17, no.1, pp.125-131. Jan 2002.

[4] T.A.Maynard, M.Fadel and N.Aouda, "Modelling of multilevel converter," IEEE Trans. Ind.Electron., vol.44, pp.356-364. Jun.1997.

[5] P.Bhagwat, and V.R.Stefanovic, "Generalized structure of a multilevel PWM Inverter," IEEE Trans. Ind. Appln, Vol.1A-19, no.6, pp.1057-1069, Nov./Dec..1983.

[6] Roozbeh Naderi, and Abdolreza rahmati, "Phase-shifted carrier PWM technique for general cascaded inverters," IEEE Trans. Power.Electron., vol.23, no.3, pp.1257-1269. May.2008.

[7] Mauricio Angulo, Pablo Lezana, Samir Kouro, Jos´e Rodr´ıguez and Bin Wu, "Level-shifted PWM for Cascaded Multilevel Inverters with Even Power Distribution" IEEE Power Electronics specialist conference, 17-21 june 2007, pp.2373-2378.

[8] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, August 2002.

Mr. T. Santosh Kumar received B.Tech Degree in Electrical and Electronics Engineering from AITAM, Tekkali, India in 2007, present he is pursuing M.tech in AITAM, Tekkali, Srikakulam, India. His research interests in Power electronics and power systems.

Dr.K.B.Madhu sahu received the B.E. Degree in Electrical Engineering from College of Engineering, Gandhi Institute of Technology & Management, Visakhapatnam, India in 1985, and the M.E Degree in power Systems from College of Engineering, Andhra University, and Visakhapatnam in 1988. He obtained his Ph.D from Jawaharlal Nehru Technological University, Hyderabad. He has 25 Years of Teaching Experience. Currently he is working as a professor & Principal in the Department of Electrical & Electronics Engineering, AITAM, Tekkali, and Srikakulam Dt. Andhra Pradesh. His research interests include gas insulated substations, high voltage engineering and power systems. He has published research papers in national and international conferences.

Sri.CH.Krishna Rao obtained B.Tech Degree in Electrical and Electronics Engineering from College of Engineering, GMRIT Rajam and Srikakulam Dt. He also obtained M.Tech in Power Electronics and Electric Drives from ASTIET Garividi, Vizayanagaram. He has 10 Years of Teaching Experience. Presently he is working as associate professor in the Department of Electrical & Electronics Engineering, A.I.T.A.M, Tekkali, and Srikakulam Dt Andhra Pradesh. He has published number of papers in journals, national and international conferences. His main areas of interest are power electronics, switched mode power supplies, electrical drives and renewable energy sources.